

<b>Notice of References Cited</b>	Application/Control No. 09/878,554	Applicant(s)/Patent Under Reexamination CHEN ET AL.	
	Examiner Joseph D. Torres	Art Unit 2133	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
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**FOREIGN PATENT DOCUMENTS**

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**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Antreich, K.J.; Schulz, M.H.; Accelerated Fault Simulation and Fault Grading in Combinational Circuits; IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 6, Issue 5, September 1987 Page(s): 704 – 712
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\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
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